AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1, 6, and 7 as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A thin film transistor (TFT) array substrate for a liquid crystal display, comprising:

an insulating substrate including a display area and a peripheral area surrounding the display area, the peripheral area including a first peripheral region arranged along a first edge of the display area and a second peripheral region arranged along a second edge of the display area;

a plurality of signal lines formed on the insulating substrate and divided into a plurality of blocks, each block including a predetermined number of signal lines;

a plurality of first repair lines formed in the first peripheral region, each crossing the signal lines of one or more of the plurality of blocks;

a second repair line formed in the first peripheral region and crossing all of the plurality of signal lines;

a plurality of third repair lines formed in the second peripheral region and connected to the first repair lines corresponding thereto, wherein each third repair line crosses the signal lines crossed by the corresponding first ~~upper~~ repair line; and

a fourth repair line formed in the second peripheral region and crossing all of the plurality of signal lines.

2. (Previously Amended) The TFT array substrate of claim 11, further comprising a plurality of first interconnection lines, each interconnecting the first repair line and the third repair line corresponding thereto.

3. (Previously Amended) The TFT array substrate of claim 2, wherein each first repair line is connected to an integrated circuit for driving the signal lines and coupled to the first interconnection line.

4. (Previously Amended) The TFT array substrate of claim 2, further comprising a plurality of second interconnection lines, each interconnecting the first repair line and the third repair line corresponding thereto.

5. (Previously Amended) TFT array substrate of claim 11, further comprising:

a fifth repair line formed in the first peripheral region and crossing the first connection members and all of the plurality of signal lines; and

a sixth repair line formed in the second peripheral region and crossing the second connection members and all of the plurality of signal lines.

6. (Currently Amended) The TFT array substrate of claim 11, wherein the signal lines of each block are connected to ~~an~~ the same integrated circuit.

7. (Currently Amended) The TFT array substrate of claim 6, wherein one of the first repair lines and one of the third repair lines cross the signal lines of two neighboring blocks.

8. (Previously Amended) The TFT array substrate of claim 7, wherein the first connection member and the second connection member are provided in each block.

9. (Previously Amended) The TFT array substrate of claim 4, wherein the first interconnection line and the second interconnection line are formed on a printed circuit board.

10. (Previously Amended) The TFT array substrate of claim 4, further comprising a signal amplifying circuit provided in the first interconnection line and the second interconnection line.

11. (Previously Presented) The TFT array substrate of claim 1, further comprising:

a plurality of first connection members, each crossing the first repair line and the second repair line; and

a plurality of second connection members, each crossing the third repair line and the fourth repair line.